Amendments to the Claims

This listing of claims replaces all prior versions, and listings, of claims in the present application.

Listing of Claims:

Claims 1-62 (canceled).

63. (New) A static memory device, comprising:

a static memory cell connected to first and second bit lines;

an input circuit, said input circuit having first and second inputs, said inputs corresponding inputting data to be written into a memory cell; and

a current generating circuit for generating first and second currents in response to received input data and applying the first and second currents to the memory cell through the bit lines, said first and second currents representing a value of the input data.

64. (New) The static memory device of claim 63, further comprising a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a write operation is not being performed.

65. (New) The static memory device of claim 63, further comprising a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a read operation or a write operation is not being performed.

66. (New) The static memory device of claim 65, wherein the predetermined voltage is smaller than a first voltage used to power the driver, but more than half of the first voltage.

67. (New) The static memory device of claim 63, wherein said current generating circuit comprises:

a first adjustable resistive element connected to a first voltage, a resistance of said first adjustable resistive element being controllable by a first control signal;

a second adjustable resistive element connected to a second voltage, a resistance of said second adjustable resistive element being controllable by a second control signal;

a first switch for switching in the resistance of the first adjustable resistive element in response to a third control signal; and

a second switch for switching in the resistance of the second adjustable resistive element in response to a fourth control signal,

wherein said first voltage is applied to said first adjustable resistive element and said second voltage is applied to said second adjustable resistive element when said third and fourth control signals are received.

68. (New) The static memory device of claim 67, further comprising a current loop generating circuit for generating the first and second control signals based on a reference voltage and a resistance of said current loop generating circuit.

69. (New) The static memory device of claim 63, further comprising:

a biasing circuit comprising:

a first resistive element coupled between a first voltage and the first bit line;

a second resistive element coupled between a second voltage and the second bit line; and

a third resistive element coupled between the first and second bit lines, wherein said resistive elements are controlled to produce a predetermined voltage level on said bit lines when a write operation is not being performed.

70. (New) The static memory device of claim 63, wherein the static memory cell is a static random access memory cell.

71. (New) The static memory device of claim 63, wherein the static memory cell is a content addressable memory cell.

72. (New) A static memory device comprising:

a static memory cell connected to first and second bit lines;

means for sensing first and second currents respectively from said first and second bit lines;

means for converting the sensed first and second currents into a voltage level representing a logical value of a content of the cell; and

means for latching the logical value until the next read operation is performed on the cell.

73. (New) The static memory device of claim 72, wherein said means for sensing comprises:

means for biasing the bit lines to a predetermined voltage;

means for discharging one of the bit lines based on the content of the memory cell; and

means for sensing the current on the bit lines.

74. (New) The static memory device of claim 72, wherein said means for sensing comprises:

means for biasing the bit lines to a predetermined voltage;

means for charging one of the bit lines based on the content of the memory cell; and

means for sensing the current on the bit lines.

75. (New) A processor system comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit comprising:

a static memory cell connected to first and second bit lines,

an input circuit, said input circuit having first and second inputs, said inputs corresponding inputting data to be written into a memory cell, and

a current generating circuit for generating first and second currents in response to received input data and applying the first and second currents to the memory cell through the bit lines, said first and second currents representing a value of the input data.

76. (New) The system of claim 75, wherein said memory circuit further comprises a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a write operation is not being performed.

77. (New) The system of claim 75, wherein said memory circuit further comprises a biasing circuit coupled to said bit lines, said biasing circuit biasing the bit lines to a predetermined voltage level when a read operation or a write operation is not being performed.

78. (New) The system of claim 77, wherein the predetermined voltage is smaller than a first voltage used to power the driver, but more than half of the first voltage.

79. (New) The system of claim 75, wherein said current generating circuit comprises:

a first adjustable resistive element connected to a first voltage, a resistance of said first adjustable resistive element being controllable by a first control signal;

a second adjustable resistive element connected to a second voltage, a resistance of said second adjustable resistive element being controllable by a second control signal;

a first switch for switching in the resistance of the first adjustable resistive element in response to a third control signal; and

a second switch for switching in the resistance of the second adjustable resistive element in response to a fourth control signal,

wherein said first voltage is applied to said first adjustable resistive element and said second voltage is applied to said second adjustable resistive element when said third and fourth control signals are received.

80. (New) The system of claim 79, wherein said memory circuit further comprises a current loop generating circuit for generating the first and second control signals based on a reference voltage and a resistance of said current loop generating circuit.

81. (New) A processor system comprising:

a processor; and

a memory circuit connected to said processor, said memory circuit comprising:

a static memory cell connected to first and second bit lines,

means for sensing first and second currents respectively from said first and second bit lines,

means for converting the sensed first and second currents into a voltage level representing a logical value of a content of the cell, and

means for latching the logical value until the next read operation is performed on the cell.

82. (New) The system of claim 81, wherein said means for sensing comprises:

means for biasing the bit lines to a predetermined voltage;

means for discharging one of the bit lines based on the content of the memory cell; and

means for sensing the current on the bit lines.

83. (New) The system of claim 81, wherein said means for sensing comprises:

means for biasing the bit lines to a predetermined voltage;

means for charging one of the bit lines based on the content of the memory cell; and

means for sensing the current on the bit lines.